

1. (Currently Amended) A bipolar transistor, comprising:
 - a substrate;
 - a semiconductor intrinsic base layer formed by blanket epitaxy on the substrate, wherein the semiconductor intrinsic base layer includes silicon germanium;
 - a collector layer formed on the substrate~~[[,]]~~ ~~wherein the semiconductor intrinsic base layer includes silicon germanium~~;
 - an emitter formed over the semiconductor intrinsic base layer, forming a junction between the semiconductor intrinsic base layer and the emitter, wherein the junction at a lateral portion of the emitter extends farther into the intrinsic base layer than the junction at a center portion of the emitter;
 - an extrinsic base formed adjacent to the lateral portion of the emitter;
 - a base electrode formed on a portion of the collector layer; and
 - an emitter electrode formed on a portion of the emitter.
2. (Previously Amended) The bipolar transistor as claimed in claim 1, wherein the emitter comprises a pedestal having a top which contacts an emitter layer.
3. (Currently Amended) The bipolar transistor as claimed in claim 1, wherein a raised extrinsic base layer is formed above the intrinsic base layer and comprises one of a highly-doped polysilicon or a highly-doped amorphouse silicon.
4. (Previously Amended) The transistor as claimed in claim 1, wherein the lateral portion has a depth in a range of approximately 20-40 nm.
5. (Cancelled)
6. (Currently Amended) The bipolar transistor claimed in claim + 3, further comprising a sidewall spacer formed between and electrically isolating the emitter and the extrinsic base layer.

7. (Previously Amended) The bipolar transistor as claimed in claim 6, wherein the sidewall spacer comprises one of a silicon nitride, a silicon dioxide, or a combination of the two.

8. (Previously Amended) The bipolar transistor as claimed in claim 7, wherein the sidewall spacer has a width in the range of 10 to 70 nanometers.

9. (Previously Amended) The bipolar transistor as claimed in claim 2, wherein the emitter layer comprises one of a polysilicon or an amorphous silicon.

10. (Previously Amended) The bipolar transistor as claimed in claim 1, wherein the emitter layer has a thickness in the range of 30 to 200 nanometers.

11. (Previously Amended) The bipolar transistor as claimed in claim 1, wherein the emitter is in-situ doped with phosphorous that minimizes drive-in and activation anneal temperatures.

Claims 12-22 (Withdrawn)

23. (Canceled)